

**IN THE CLAIMS:**

1. (Currently Amended) A method for forming MOS transistor gate dielectrics, comprising:
  - providing a semiconductor substrate;
  - forming a first dielectric layer on said semiconductor substrate;
  - performing a first plasma nitridation of said first dielectric layer;
  - removing said first dielectric from a region of said substrate;
  - forming a second dielectric layer on said semiconductor substrate in said region from which said first dielectric layer ~~were~~ was removed; and
  - simultaneously performing a second plasma nitridation of said second dielectric layer and said first dielectric layer.
2. (Original) The method of claim 1 wherein said first dielectric layer comprises silicon oxide.
3. (Original) The method of claim 2 wherein said second dielectric layer comprises silicon oxide.
4. (Original) The method of claim 1 wherein said second dielectric layer has a final nitrogen concentration of 5 to 15 atomic percent following said first and second plasma nitridation.

5. (Original) The method of claim 4 wherein said first dielectric layer has a nitrogen concentration of 5 to 20 atomic percent following said second plasma nitridation.

6. (Previously Presented) A method for forming integrated circuit MOS transistors, comprising:

providing a semiconductor substrate;

forming a first silicon oxide layer;

performing a plasma nitridation process on said first silicon oxide layer forming a first plasma nitrided oxide layer;

removing said first plasma nitrided oxide layer from regions of said substrate; and

forming a second plasma nitrided oxide layer on said semiconductor substrate in said regions from which said first plasma nitrided oxide layer was removed.

7. (Original) The method of claim 6 wherein said forming said second plasma nitrided oxide layer comprises:

forming a second silicon oxide layer in said regions from which said first plasma nitrided oxide layer was removed; and

performing a second plasma nitridation process on said second oxide layer and said first plasma nitrided oxide layer.

8. (Original) The method of claim 7 wherein said first plasma nitrided oxide layer comprises 5 to 15 atomic percent of nitrogen.

9. (Withdrawn) Integrated circuit MOS transistors, comprising:

a semiconductor substrate;

a first plasma nitrided oxide layer formed on a first region of said semiconductor substrate;

a second plasma nitrided oxide layer formed on a second region of said semiconductor substrate wherein said second plasma nitrided oxide layer is formed using dual nitridation processes;

a first transistor gate formed on said first plasma nitrided oxide layer; and

a second transistor gate formed on said second plasma nitrided oxide layer.

10. (Withdrawn) The integrated circuit MOS transistors of claim 9 where said first plasma nitrided oxide layer comprises 5 to 20 atomic percent of nitrogen.

11. (Withdrawn) The integrated circuit MOS transistors of claim 10 where said second plasma nitrided oxide layer comprises 5 to 15 atomic percent of nitrogen.